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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,305	01/23/2004	Jin Ping Liu	CS03-054	6526

7590 05/10/2005

STEPHEN B. ACKERMAN
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/763,305	LIU ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-25* is/are allowed.

6)☒ Claim(s) *1-4 and 6-14* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 18, 2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 3, 7, 8, 9, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Fitzgerald, US 6,646,322.

Regarding claims 1 – 3, 7, 9 and 13, Fitzgerald teaches a method of forming a semiconductor alloy layer featuring the use of only one underlying graded semiconductor alloy layer, comprising the steps of:

- providing a semiconductor substrate of silicon 102 (see Fig. 1)
- without the use of a seed layer growing a graded, first semiconductor alloy layer 104 directly on said semiconductor substrate 102, wherein the content of a

component (Si) of said graded, first semiconductor alloy layer (Si –Ge) is decreased as the growth of said graded, first semiconductor alloy layer progresses;

- growing a non- graded, second semiconductor alloy layer (Si –Ge)106 on said graded, first semiconductor alloy layer 104, wherein the content of said component (Si) in said second semiconductor alloy layer is uniform, and wherein said second semiconductor alloy layer is in a strain relaxed form (see Fig. 1); and
- forming a semiconductor layer of Si on said relaxed second semiconductor alloy layer, wherein said semiconductor layer is comprised with tensile strain (see Figs. 5A – 5D). Also see descriptions in column 1, lines 30 – 33 and in column 3, lines 38 – 47.

Regarding claim 8, Fitzgerald teaches the composition of the component in the graded alloy layer ranging between 0 – 50 wt% with respect to Fig. 1.

Regarding claim 12, Fitzgerald teaches the composition of the component in the second semiconductor alloy layer ranging between 20 – 100 wt% with respect to Fig. 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 4, 6, 10, 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fitzgerald, US 6,646,322 in view of Leitz, US 2004/0087117.

Regarding claims 4, 6 and 10, Fitzgerald fails to teach the deposition process of the layers and the thickness of the graded layer.

Leitz teaches forming the graded and relaxed silicon – germanium semiconductor alloy layer by using silane and germane via LPCVD process and a thickness between 300 – 1000 Angstroms in paragraphs 56 and 73 for the benefit of growing high quality device layer in paragraph 7.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Fitzgerald and form the graded and relaxed silicon – germanium semiconductor alloy layer by using silane and germane via LPCVD process and a thickness between 300 – 1000 Angstroms for the benefit of growing high quality device layer as taught by Leitz in paragraph 7

Regarding claims 11, Fitzgerald fails to teach the thickness of the second semiconductor alloy layer.

Leitz teaches forming the relaxed silicon – germanium semiconductor alloy layer to a thickness between 2000 – 10,000 Angstroms in paragraph 63 for the benefit of growing high quality device layer in paragraph 7.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Fitzgerald and form the relaxed silicon – germanium semiconductor alloy layer to a thickness between 2000 – 10,000 Angstroms for the benefit of growing high quality device layer as taught by Leitz in paragraph 7.

Regarding claims 14, Fitzgerald fails to teach the deposition process of the semiconductor layer and the thickness of the semiconductor layer.

,Leitz teaches forming the silicon semiconductor layer via LPCVD using silane in paragraphs 56 – 58 and a thickness between 100 – 200 Angstroms in paragraph 67 for the benefit of growing high quality device layer in paragraph 7.

Therefore, it would have been obvious to one with ordinary skill in the art at the

time of the invention to modify Fitzgerald and form the silicon semiconductor layer via LPCVD using silane and a thickness between 100 – 200 Angstroms for the benefit of growing high quality device layer as taught by Leitz in paragraph 77.

Allowable Subject Matter

8. Claims 15 – 25 are allowed.

9. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the allowance and the indication of allowable subject matter:

These claims recite, inter alia, a method of forming tensile strained silicon layer on a relaxed Si – Ge layer on a semiconductor substrate without the use of a seed layer comprising the step of growing a graded first semiconductor alloy Si - Ge layer directly on the semiconductor substrate, wherein the content of Ge of the graded first semiconductor alloy layer is decreased as the growth of said graded semiconductor alloy layer progresses. The art of record does not disclose or anticipate the above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
May 6, 2005

Primary Examiner